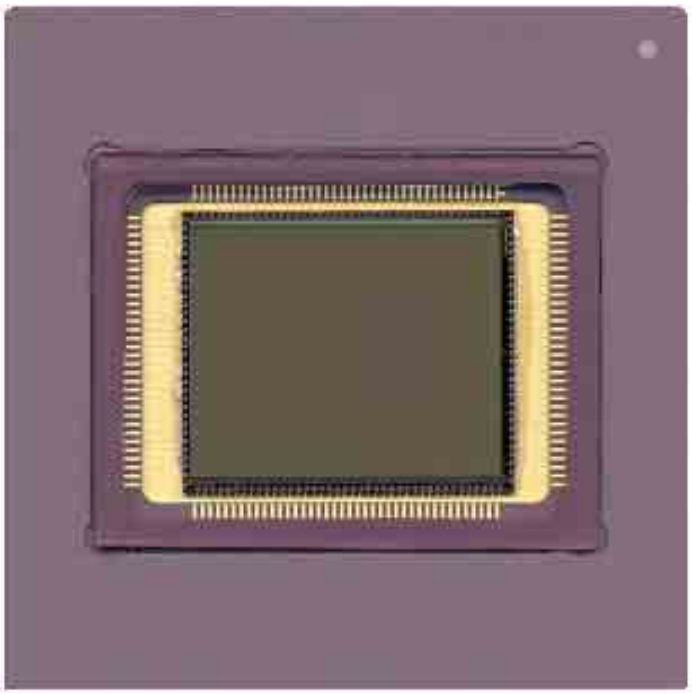
LUPA1300

High speed CMOS image sensor
Data sheets



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1 Introduction

This document describes the interfacing and the driving of the image sensor LUPA, which is a 1280 by 1024 CMOS pixel array working at 450 frames/sec. It allows the user to develop a camera system based on the described timing and interfacing.

2 General description

The LUPA sensor is a 1280 by 1024 active pixel sensor with **synchronous** shutter, processed in the Tower in TS50 process. The pixel size is 14 * 14 um2 and the sensor is designed to achieve a fame rate of 450 frames/sec at full resolution. This high frame rate can be achieved by 16 parallel output amplifiers each working at 40MHz pixel rate. In the following sections the different modules of the image sensor are discussed more into detail.

2.1 CMOS image sensor architecture

The image sensor consists of the pixel array, the column readout electronics, X-and Y addressing, on chip drivers, the output amplifiers and some logic.

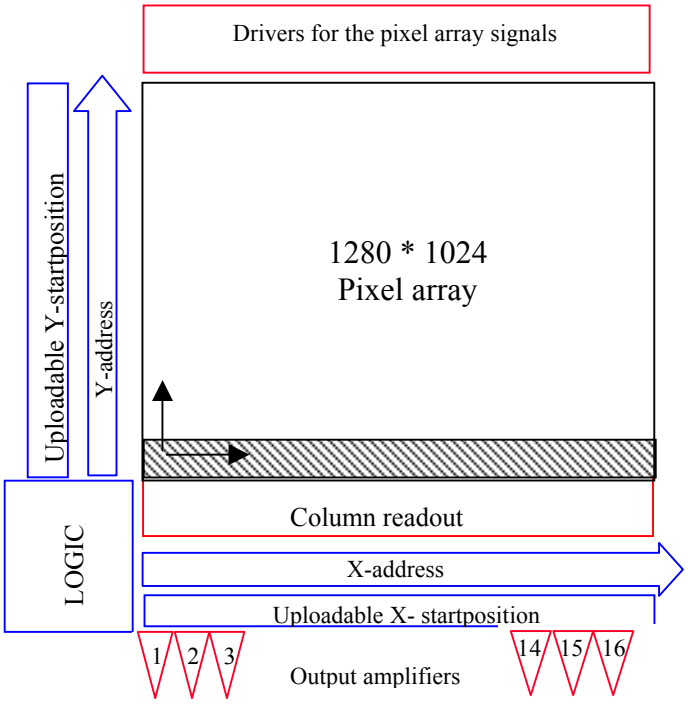


Figure 1 : architecture of the LUPA sensor

Figure 1 shows a schematic representation of the image sensor on which the different modules are displayed.
The image core is a pixel array of 1280 * 1024 pixels each of 14 *14 µm2 in size. The readout is from bottom left to top right. To obtain a frame rate of 450 frames/sec for this resolution, we have chosen 16

output amplifiers each capable of driving an output capacitance of 20 pF at 40MHz.
The column readout amplifiers bring the pixel data to the output amplifiers. The logic and the x- and y addressing controls the image sensor so that progressive scan and windowing is possible. Extra pixel array drivers are foreseen at the top of the image sensor to control the global pixel array signals.

2.2 Pixel architecture

The active pixels allow synchronous shutter "i.e. all pixels are illuminated during the same integration time, starting from the same moment in time. After a certain integration time, the pixels are readout sequentially. Readout and integration are in parallel, which means that when the image sensor is readout, the integration time for the next frame is ongoing. This feature requires a memory element inside the pixel, which affects the maximum fill factor. A schematic representation of the pixel is given in figure 2.

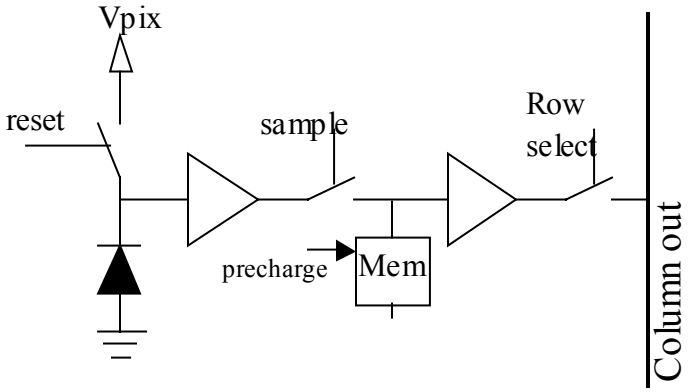


Figure 2 : schematic representation of the synchronous pixel as used in the LUPA design
The signals mentioned in figure 2 are the internal signals, generated by the internal drivers, required to have the synchronous shutter feature.

The photodiode is designed to obtain a sensitivity as high as possible for a dynamic range of at least 60dB. Consequently the photodiode capacitance is 10fF @ the output, resulting in a S/N of more than 60dB as the rms noise level is within the expectation of 45 noise electrons.

2.3 Column readout amplifiers

The column readout amplifiers are the interface between the pixels and the output amplifiers. The pixels in the array are selected line by line and the pixels of the selected line are connected to the column readout amplifiers, which bring the pixel data in the correct format to the output amplifiers.
To obtain a high frame rate, the complexity and the number of stages in the column readout amplifiers must be minimized, so that the power dissipation remains as low as possible, but also to minimize the row blanking time. Figure 3 is a schematic representation of the column readout structure. It consists of 2 parts. The first part is a module that reduces the row blanking time. The second part shifts the signal to the correct level for the output amplifiers and allows multiplexing in the x-direction.
From the moment that a new row is selected, the pixel data of that row is placed onto the columns of the pixel array. These columns are long lines and have a large parasitic capacitance. As the pixel is small, it is not possible to match the transistor inside the pixel, which drives this column. Consequently, the first module in the column readout amplifiers must solve the mismatch between the pixel driver and the large column capacitance. In this image sensor we have implemented 2 methods to obtain a short line blanking time. The first baseline method is a straight forward track and hold method. The second method is based on a new technique, which brings the columns to a reference level before the row is selected. This technique results in a shorter row blanking time (< 200nsec), reduced power dissipation and an increase voltage swing.

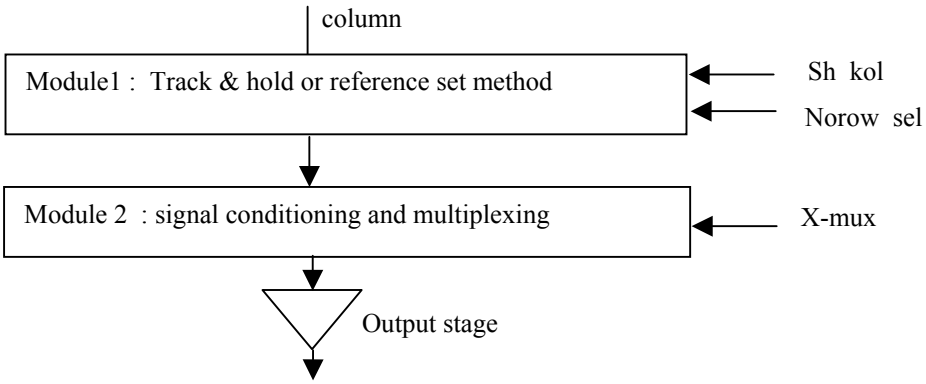


Figure 3 : Schematic representation of the column readout structure.

2.4 Output amplifiers

16 output amplifiers each capable of working at 40MHz pixel rate are placed equidistant on the bottom of the image sensor. These output amplifiers are required to obtain a frame rate of 450 frames/sec. A single output stage, not only to reduce power, but also to achieve the required pixel rate is designed. Figure 4 is a schematic representation of this module and figure 5 shows output curves one can expect from these output amplifiers.

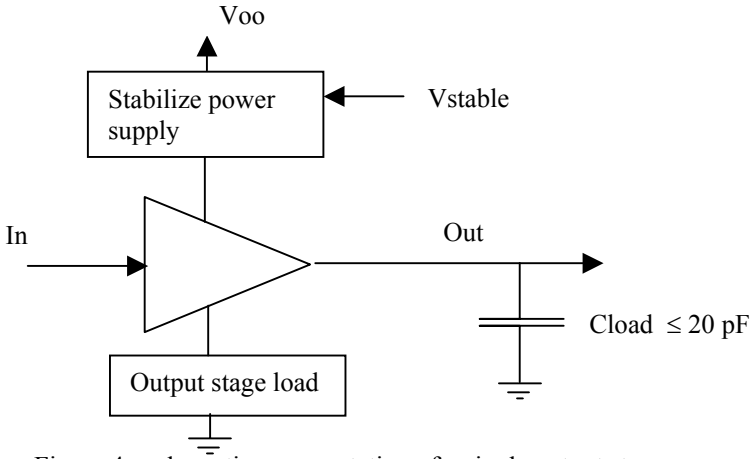


Figure 4 : schematic representation of a single output stage.

Each output stage is designed to drive a load of 20pF at a pixel rate of 40MHz. The load in the output stage determines this pixel rate. In case the load capacitance is less than 20pF, the load in the output stage can increase, resulting in less power dissipation of the output stages and consequently of the whole sensor. Additionally, decreasing the load of the output stage allows having more current available for the output stage to charge or discharge the load capacitance to obtain a higher pixel rate.
To avoid variations on the supply voltage to be seen on the output signal, a special module to stabilize the power supply is required. This module that requires an additional supply voltage (Vstable) allows variation on the supply voltage Voo without being seen on the output signal.
One can also choose to have a passive load of chip instead of the active output stage load. This deteriorates the linearity of the output stages, but decreases the power dissipation, as the dissipation in the load is external.

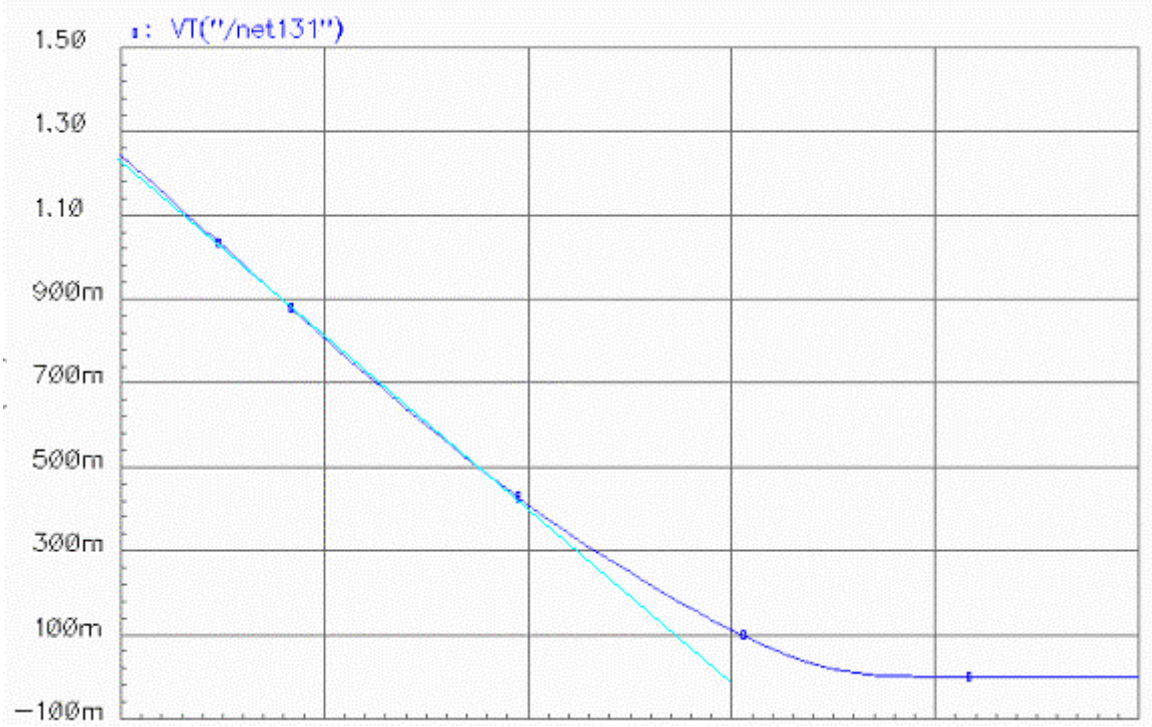


Figure 5 : output voltage as a function of light. The cyan line is a linear fit between 1.2 and 0.3V.

As one can see from figure 5, the output signal ranges between 1.2 V (dark) to 0 V (saturation) and is linear till around 300mV, (below which is approaches a logarithmic response). We expect in principle a linear range of 600 – 800mV on a total signal range of 1V.

2.5 X-Y addressing and windowing

The pixel array is readout by means of programmable X and Y shift registers. The pixel array is scanned line by line and column by column. The starting point in X and Y is defined individually for each register and is determined by the address downloaded by the Serial – Parallel Interface (SPI). Both registers work in the same way. A sync pulse that sets the address pointer to the starting address of each register, initializes them. A clock pulse for the x- and y-shift register shifts the pointer individually and makes sure that the sequential selection of the lines and columns is correct.

2.6 Temperature reference

On the same image sensor we have foreseen a module to verify the temperature on chip and the variation of the output voltage due to a temperature variation. This module contains a copy of the complete signal path, including a blind pixel, the column amplifiers and an output stage. It DC response may serve a temperature calibration for the real signal. The temperature functionality is given in figure 6. Between room temperature and 60 °C we see a voltage variation of about 50mV.
Note that the simulations are done at a fixed voltage supply of 5V. Due to different applied supply voltages, as there are: Vreset, Vmem, Vpix… an offset between the output voltage of the temperature sensor and the output of a black signal of the pixel array can occur. Depending on the working conditions of the image sensor one can fine-tune the temperature sensor with its voltage supply. In case one has a 6V signal for reset and a 4-6V signal for Vmem, a supply voltage of 5.5V for the temperature sensor will result in a closer match between this temperature sensor and the black level of the image sensor. Changing the

supply voltage of the temperature sensor results only in a shift of the output voltage.

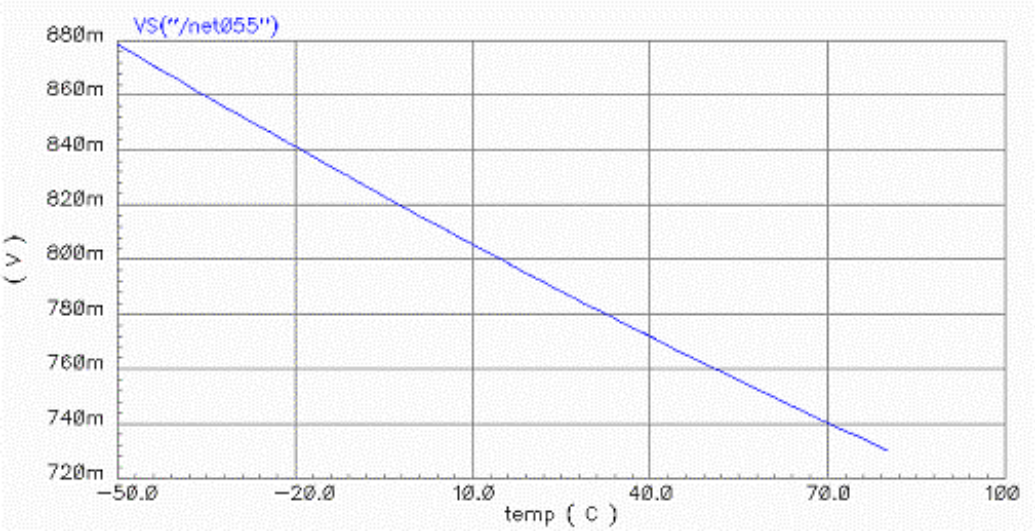


Figure 6 : temperature reference voltage variation as function of the temperature (Vsupply : 5V)

3 Specifications

3.1 General specifications

Parameter	Value
Pixel pitch	14 * 14 μm^2
Resolution	1280 * 1024
Frame rate	450 frames/sec@ 40MHz output
die size	19.2 * 16.2 mm^2
Readout sequence	Progressive scan
Shutter type	Synchronous with variable integration time
Windowing	Programmable via SPI
Number of outputs	16
Color filter pattern	Bayer (first pixel = red)
Package	Pin grid array 145 pins

Table 1 : general specifications of the LUPA sensor

3.2 Electrical characteristics

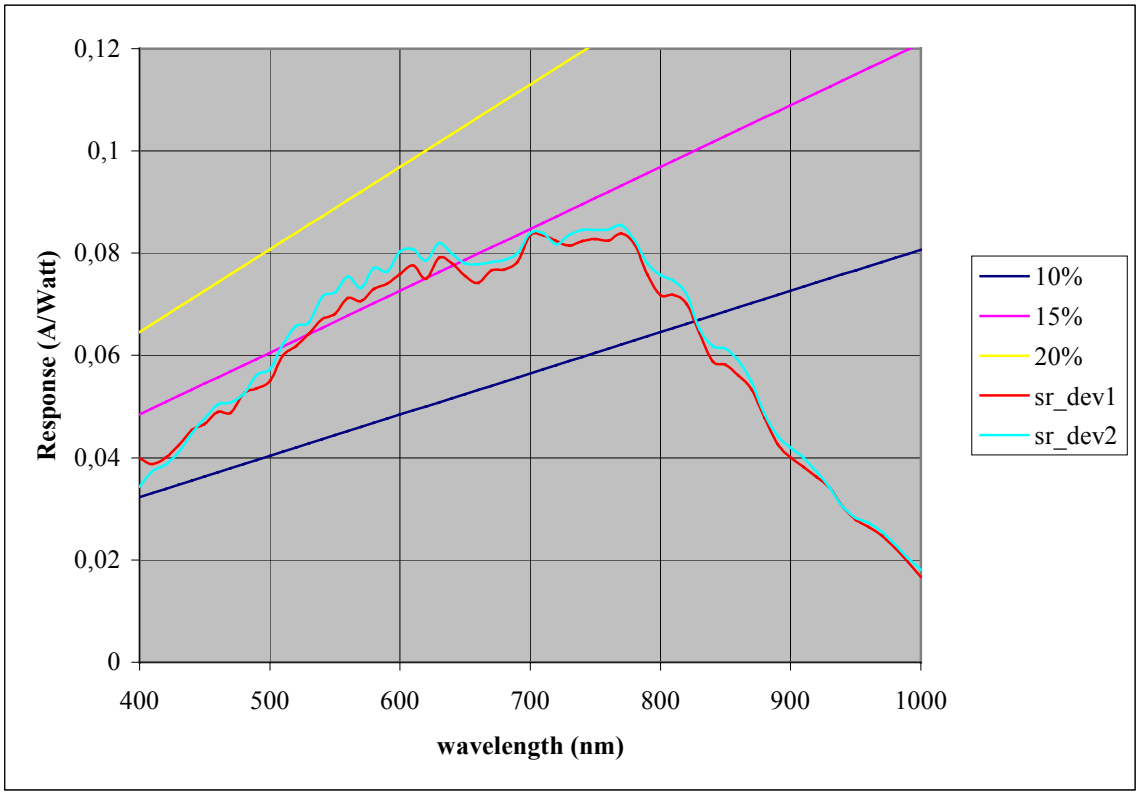
Parameter	conditions	Minimum	typical	maximum	unit
Power supply	General supply		5		V
Power dissipation			500	700	mWatt
# output amplifiers			16		
Pixel rate	@ 1 output		40	60	MHz
Frame rate	@ full frame		450	675	Fr/sec.
X clock			20	30	MHz
Y-Clock			0.65	1.3	MHz
Photodiode capacitance	@ the output		10		fF
Sensitivity	@ the output		16		µV/e
Output voltage		0.6	1	1.3	V
Full well charge			60.000		e-
Temporal noise	Dark environment T=21°C		45		e-
Dynamic range			1330 or 62dB		
Line blanking time	Mode SH Mode norowsel	250 150	300 250		nsec nsec

Table 2 : electrical specifications of the LUPA sensor

3.3 Optical characteristics

Parameter	conditions	minimum	Typical	maximum	unit
Fill factor	100% - metal and polycide coverage		50		%
Peak fill factor * spectral response	λ=700nm		0.08		A/W
Fill factor * peak QE	λ=700nm		15		%
FPN			5		%
PRNU	Half saturation		10		%
Optical crosstalk	Pixel to pixel		15		%

Table 3 : optical specifications of the LUPA sensor



4 Pin configuration

The LUPA sensor will be packed in a PGA package with 145 pins. Each bondpad consists of 2 pad openings, one for wafer probing and one for bonding. Table 4 gives an overview of the pin names and their functionality.

Pin	fp	Name	Function	description
B3	1	n.c.		Not connected
C3	2	n.c.		
D3	3	Voo	Supply 5V	Supply voltage output stages : 5V
A2	4	Gnd	Ground	Ground of the sensor
B2	5	Out1	Analog out	Output 1
E3	6	Voo	Supply 5V	Supply voltage output stages : 5V
C2	7	Out2	Analog out	Output 2
D2	8	Gnd	Ground	Ground of the sensor
E2	9	Out3	Analog out	Output 3
A1	10	Voo	Supply 5V	Supply voltage output stages : 5V
F3	11	Out4	Analog out	Output 4
F2	12	Gnd	Ground	Ground of the sensor
B1	13	Out5	Analog out	Output 5
C1	14	Voo	Supply 5V	Supply voltage output stages : 5V
D1	15	Out6	Analog out	Output 6
G3	16	Gnd	Ground	Ground of the sensor
E1	17	Out7	Analog out	Output 7
G2	18	Voo	Supply 5V	Supply voltage output stages : 5V
F1	19	Out8	Analog out	Output 8
G1	20	Gnd	Ground	Ground of the sensor
H3	21	Out9	Analog out	Output 9
H2	22	Voo	Supply 5V	Supply voltage output stages : 5V
H1	23	Out10	Analog out	Output 10
J1	24	Gnd	Ground	Ground of the sensor
J2	25	Out11	Analog out	Output 11
J3	26	Voo	Supply 5V	Supply voltage output stages : 5V
K1	27	Out12	Analog out	Output 12
K2	28	Gnd	Ground	Ground of the sensor
L1	29	Out13	Analog out	Output 13
K3	30	Voo	Supply 5V	Supply voltage output stages : 5V
L2	31	Out14	Analog out	Output 14
M1	32	Gnd	Ground	Ground of the sensor
N1	33	Out15	Analog out	Output 15
L3	34	Voo	Supply 5V	Supply voltage output stages : 5V
M2	35	Out16	Analog out	Output 16
P1	36	Gnd	Ground	Ground of the sensor
N2	37	Voo	Supply 5V	Supply voltage output stages : 5V
M3	38	n.c.		
P2	39	n.c.		
N3	40	Gnd	Ground	Ground of the sensor
N4	41	Voo	Supply 5V	Supply voltage output stages : 5V
N5	42	Vstable	Supply 5V	Supply voltage to stabilize output stages : 5.5V
P3	43	Load_out	Biasing	Analog bias for output amplifiers 27KΩ to Voo and capacitor of 100nF to ground

P5	44	Dc_black	Testpin 6	dc-black signal required to characterise the output stages
P4	45	Vdd	Supply 5V	Supply voltage digital modules : 5V
Q1	46	Gnd	Ground	Ground of the sensor
N6	47	Vdda	Supply 5V	Supply voltage analog modules : 5V
P6	48	Gnd	Ground	Ground of the sensor
Q2	49	Vpix	Supply 5V	Supply voltage pixel array : 5V
Q3	50	Eos_x	Digital I/O	End of scan signal of the x-register : active high pulse indicates the end of the shift register is reached
Q4	51	Nsf_load	Biasing	Analog bias for column stages : 180KΩ to Vdda and capacitor of 100nF to ground
N7	52	Psf_load	Biasing	Analog bias for column stages : 240KΩ to gnd and capacitor of 100nF to Vdda
P7	53	Col_load	Biasing	Analog bias for column stages : 2MΩ to Vdda and capacitor of 100nF to ground
Q5	54	Pre_load	Biasing	Analog bias for column stages : 10KΩ to Vdda and capacitor of 100nF to ground
Q6	55	n.c.		
Q7	56	Array_diode	Testpin 3	Array of photodiodes as designed in pixel : 10 * 5
N8	57	Full_diode	Testpin 4	Full diode with same array as array diode : 140 * 70 μm^2
P8	58	Temp_diode_p	Testpin 1	Temperature diode p side
Q8	59	Temp_diode_n	Testpin 2	Temperature diode n side
Q9	60	n.c.		
P9	61	n.c.		
N9	62	n.c.		
Q10	63	n.c.		
Q11	64	n.c.		
Q12	65	n.c.		
P10	66	n.c.		
N10	67	n.c.		
Q13	68	n.c.		
P11	69	Vpix	Supply 5V	Supply voltage pixel array : 5V
P12	70	Gnd	Ground	Ground of the sensor
N11	71	Vddr	Supply 5V	Supply voltage of the logic for the drivers : 5V
N12	72	n.c.		
P13	73	Vmem_l	Supply	Voltage supply for Vmemory drivers : 3V- 5V (typ: 4.5V)
N13	74	Vmem_h	Supply	Voltage supply for Vmemory drivers : 4V- 6V (typ. 6V)
M13	75	Vres_ds	Supply	Voltage supply for reset double sloped drivers : 4V – 5V
Q14	76	Vres	Supply	Voltage supply for reset drivers : 5V – 6V (typ 6V)
P14	77	Gnd_res	Ground_ab	Ground anti-blooming : 0 – 1V
L13	78	n.c.		
N14	79	n.c.		
M14	80	n.c.		
L14	81	n.c.		
Q15	82	n.c.		
K13	83	n.c.		
K14	84	n.c.		
P15	85	n.c.		
N15	86	n.c.		

M15	87	n.c.		
J13	88	n.c.		
L15	89	n.c.		
J14	90	n.c.		
K15	91	n.c.		
J15	92	n.c.		
H13	93	n.c.		
H14	94	Gnd	Ground	Ground for temperature module
H15	95	Temp	Testpin 5	Dark level signal as function of temperature (figure 8)
G15	96	Vdd	Supply 5V	Supply voltage temperature module : 5V
G14	97	n.c.		
G13	98	n.c.		
F15	99	n.c.		
F14	100	n.c.		
E15	101	Reset_ds	Digital I/O	Double slope reset of the pixels: active high pulse
F13	102	Reset	Digital I/O	Reset signal of the pixels : active high pulse
E14	103	Mem_hl	Digital I/O	Control of Vmemory signal : 5V: Vmem_h, 0V : Vmem_l
D15	104	Sample	Digital I/O	Samples the photodiode voltage onto the memory cell inside each pixel : active high pulse
C15	105	Precharge	Digital I/O	Precharge the memory cell inside the pixel : active high pulse
E13	106	Eos_y	Digital I/O	End of scan signal of the y-register : active high pulse indicates the end of the shift register is reached
D14	107	Gnd_Res	Ground_ab	Ground for the reset drivers. Can be used as anti-blooming by applying 1V instead of 0V
B15	108	Vres	Supply	Voltage supply for reset drivers : 5V – 6V (typ: 6V)
C14	109	Vres_ds	Supply	Voltage supply for reset double sloped drivers : 4V – 5V
D13	110	Vmem_h	Supply	Voltage supply for Vmemory drivers : 5V- 6V (typ: 6V)
B14	111	Vmem_l	Supply	Voltage supply for Vmemory drivers : 3V- 5V (typ: 4.5V)
C13	112	Vddr	Supply 5V	Supply voltage of the logic for the drivers : 5V
C12	113	Vpix	Supply 5V	Supply voltage pixel array : 5V
C11	114	Vdd	Supply 5V	Supply voltage digital modules : 5V
B13	115	Gnd	Ground	Ground of the sensor
B11	116	n.c.		
B12	117	n.c.		
A15	118	n.c.		
C10	11	n.c.		

	9			
B10	120	n.c.		
A14	121	n.c.		
A13	122	n.c.		
A12	123	n.c.		
C9	124	n.c.		
B9	125	n.c.		
A11	126	Load_addr	Digital I/O	Loads the address into the serial parallel interface (SPI)
A10	127	Address	Digital I/O	Serial address to be downloaded into the SPI
A9	128	Clock_spi	Digital I/O	Clock for the SPI
C8	129	Decy_load	Digital I/O	Bias for y address register : 27KΩ to ground and capacitor of 100nF to Vdd
B8	130	Sync_y	Digital I/O	Synchronisation of y-address register : active high
A8	131	Clock_y	Digital I/O	Clock of y-address register
A7	132	Norow_sel	Digital I/O	Control signal for Norow_sel mode to reduce row blanking time : active low
B7	133	Sh_col	Digital I/O	Control signal for Sh_col mode to reduce row blanking time : active low (baseline method) : active low
C7	134	Pre_col	Digital I/O	Additional control signal for reducing the row blanking time
A6	135	Sync_x	Digital I/O	Synchronisation of the x-address register : active high
A5	136	Clock_x	Digital I/O	Clock of the x-address register
A4	137	Decx_load	Biasing	Bias for x address register : 27KΩ to ground and capacitor of 100nF to Vdd
B6	138	Black	Digital I/O	Controls black test function of the output stages : active high
C6	139	Sel_active	Digital I/O	set the output stages active or in standby mode : active low
A3	140	Vdd	Supply 5V	Supply voltage digital modules : 5V
B5	141	Gnd	Ground	Ground of the sensor
B4	142	Vdda	Supply 5V	Supply voltage analog modules : 5V
C5	143	Gnd	Ground	Ground of the sensor
C4	144	Voo	Supply 5V	Supply voltage output stages : 5V

Table 4 : pin description of the assembled LUPA sensor in the PGA 144 package.

One can distinguish the different signals into different groups :

- Power supplies and grounds
- Biasing and analog signals
- Pixel array signals
- Digital signals
- Test signals

4.1 Power supplies and grounds

Every module on chip, as there are: column readout, output stages, digital modules, drivers, …, has its own power supply and ground. Off chip the grounds can be combined, but not all power supplies may be combined. This results in a huge amount of power supplies, but is required to reduce electrical crosstalk and to improve shielding.
On chip we have the ground lines also separately for every module to improve shielding and electrical crosstalk between them. The only special ground is "Gnd_res", which can be used to remove the blooming if any and which can improve optical crosstalk.
An overview of the supplies is given in table 5. The power supplies related to the pixel array signals are described in the paragraph concerning the pixel array signals.

Name	Max current	Typ.	Max	Description
Vdda	50mA	5V		Power supply column readout module
Vdd	20mA	5V		Power supply digital modules
Voo	70mA	5V		Power supply output stages
Vstable	5mA	5.5V	6V	Power supply output stages. Decouples noise on the Voo supply from the output signal.
Vpix	200mA	5V	6V	Power supply pixel array.
Vddr	20mA	5V		Power supply logic for drivers

Table 5 : power supplies used in the LUPA design

The maximum currents mentioned in table 5 are peak currents. The power supplies need to be able to deliver these currents. Especially the maximum supply current for Vpix
It is important to notice that we don't do any power supply filtering on chip and that noise on these power supplies can contribute immediately to the noise on the signal. Especially the voltage supplies Vpix and Vdda are important to be well noise free. With respect to the power supply Voo, a special decoupling is used, for which an additional power supply Vstable is required.

4.2 Biasing and analog signals

Besides the biasing signals, the only analog signals are the output signals Out1 – Out16. Each output signal is analog with respect to the voltage level, but is discrete in time. This means that on the speed of Clock_x, the outputs change to a different level, depending on the illumination of the corresponding pixels.

The biasing signals determine the speed and power dissipation of the different modules on chip. These biasing signals have to be connected trough a resistor to ground or power supply and should be decoupled with a capacitor. If the sensor is working properly, each of the biasing signals will have a dc-voltage depending on the resistor value and on the internal circuitry. These dc-voltages can be used to check the operation of the image sensor. Table 6 gives the different biasing signals, the way they should be

connected, and the expected dc-voltage. Due to small process variations, these dc-voltages change from chip to chip and 10% variation is possible.

Signal	Comment	Expected dc-level
Pre_load	Connect with 10KΩ to Vdda and capacitor of 100nF to Gnd	1.4V
Col_load	Connect with 2MΩ to Vdda and capacitor of 100nF to Gnd	1.1V
Psf_load	Connect with 240KΩ to Gnd and capacitor of 100nF to Vdda	3.9V
Nsf_load	Connect with 180KΩ to Vdda and capacitor of 100nF to Gnd	1.3V
Load_out	Connect with 27KΩ to Voo and capacitor of 100nF to Gnd	1.2V
Decx_load	Connect with 27KΩ to Gnd and capacitor of 100nF to Vdd	3.9V
Decy_load	Connect with 27KΩ to Gnd and capacitor of 100nF to Vdd	3.9V

Table 6 : overview of biasing signals

Each resistor controls the speed and power dissipation of the corresponding module, as this resistor determines the current required to charge and / or discharge internal nodes inside the module. It is possible that certain internal nodes are smaller or larger than calculated and that a larger or smaller resistor can be used. In fact, one should try to have the largest resistor as possible to minimise power dissipation although still receiving the required speed. During testing of the prototypes, this will be investigated into detail.
A decoupling with a small capacitor is advisable to reduce the HF noise onto the analog signals. Only the capacitor on the Pre_load signal can be omitted.

4.3 Pixel array signals

Figure 2 in paragraph 2.2 is a schematic representation of the pixel as used in the LUPA design. The applied signals to this pixel are: reset, sample, Precharge, Vmemory, row select and Vpix. These are internal generated signals derived by on chip drivers from external applied signals. Consequently it is important to understand the relation between both internal and external signals and to understand the operation of the pixel.
The timing of the pixel is given in figure 7 in which only the internal signals are given.

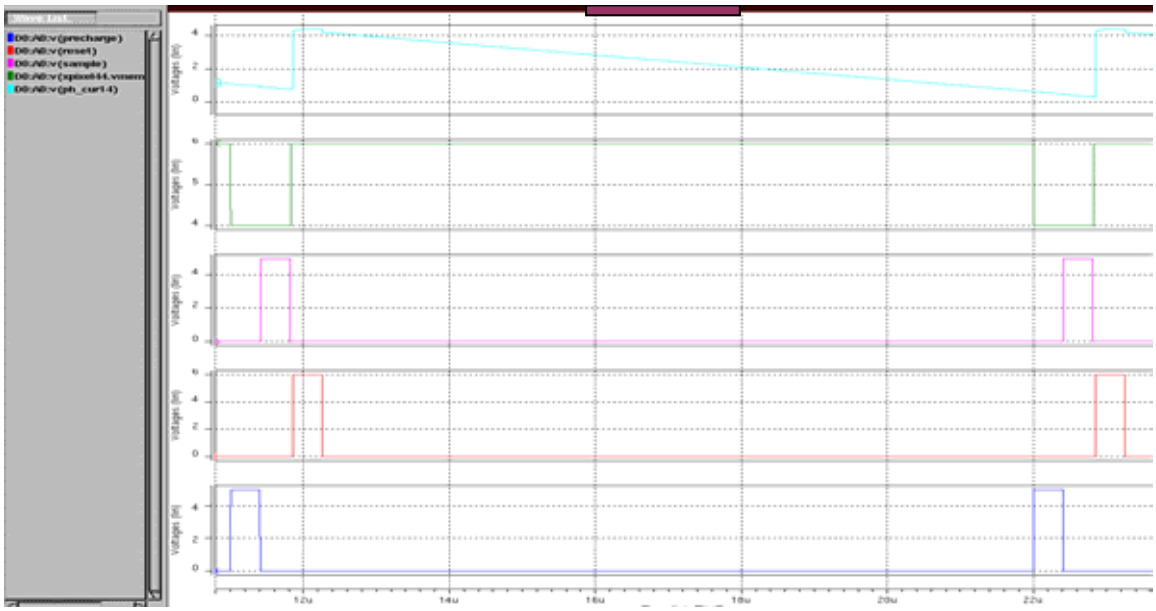


Figure 7 : Internal timing of the pixel. The signals from top to bottom are : Integration slope on the photodiode node, Vmemory, sample, reset and Precharge.

The top signal in figure 7 is the voltage onto the photodiode, which shows an integration slope due to a certain "simulated" illumination. The integration time ends on the rising edge of reset and starts on the falling edge of reset. In this example we have an integration time of about 11µsec. At the end of the integration time, the information on the photodiode node needs to be sampled and stored onto the pixel memory, required to allow synchronous shutter. To do this, we need the signals "Precharge" and "Sample". "Precharge" resets the pixel memory and "Sample" places the pixel information onto the pixel memory. Once this information stored, the readout of the pixel memories can start in parallel with a new integration time. An additional signal "Vmem" is needed to obtain a larger output swing.
Except from Vpix power supply, drivers generate the other pixel signals on chip. The external signals to obtain the required pulses consist of 2 groups. One is the group of digital signals to indicate when the pulse must occur and the other group are dc-supply lines indicating the levels of the pulses. Table 7 tries to summarize the relation between the internal and external pixel array signals

Internal signal	Vlow	Vhigh	External control signal	Low dc level	High dc level
Precharge	0	5V	Precharge	Gnd	Vddr
Sample	0	5V	Sample	Gnd	Vddr
Reset	0V	4 – 6V	Reset & Reset_ds	Gnd_res	Vres & Vres_ds
Vmemory	4.5V	6V	Mem_hl	Vmem_l	Vmem_h

Table 7: overview of the internal and external pixel array signals.

The Precharge and Sample signals are the most straightforward signals. The internal signal Vmemory is a signal that switches between a low voltage (3.5 – 5.5V) and a high voltage (5-6V). The signal Mem_hl controls the applied level and the power supply lines Vmem_l and Vmem_h determine the low and high dc-levels.
The Reset signal is due to the dual slope technique a little more complex. In case the dual slope is not used, the reset signal is straightforward generated from the external reset pulse. In this case the supply voltage Vres determines the level to which the pixel is resetted.
In case the dual slope operation is desired, one needs to give a second pulse to a lower reset level during integration. This can be done by the control signal Reset_ds and by the power supply Vres_ds that defines the level to which the pixel has to be resetted. Figure 8 shows the relation between the internal and external signals Sample and Precharge. Figure 9 shows the same as figure 8 but for the Vmemory signal. Figure 10 is for the reset signals.

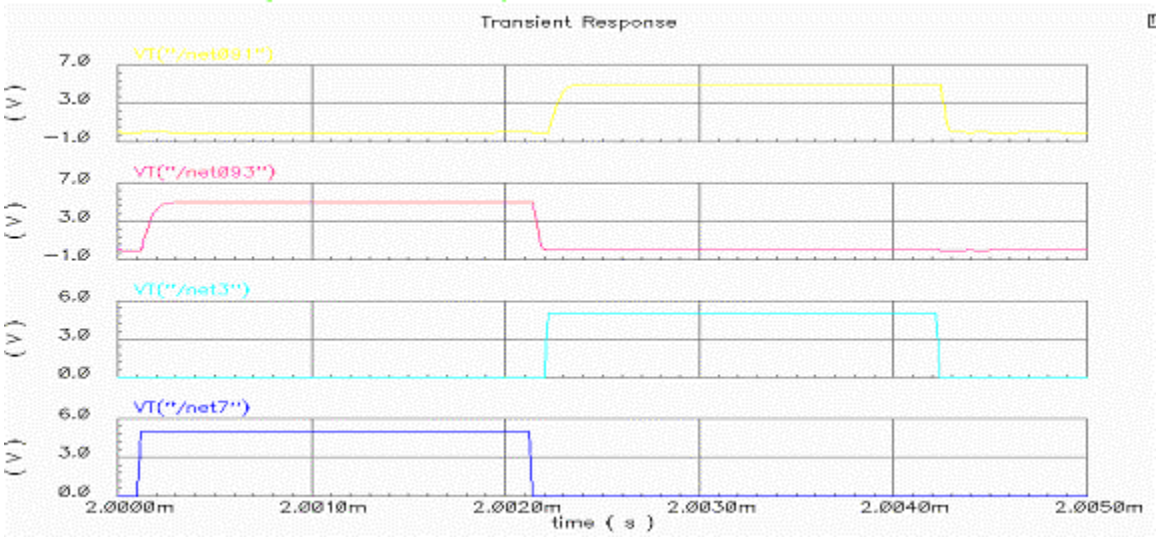


Figure 8 : relation between internal and external Sample and Precharge signals. Curves from top to bottom : internal signal Sample, Internal signal Precharge, external signal Sample, external signal Precharge.

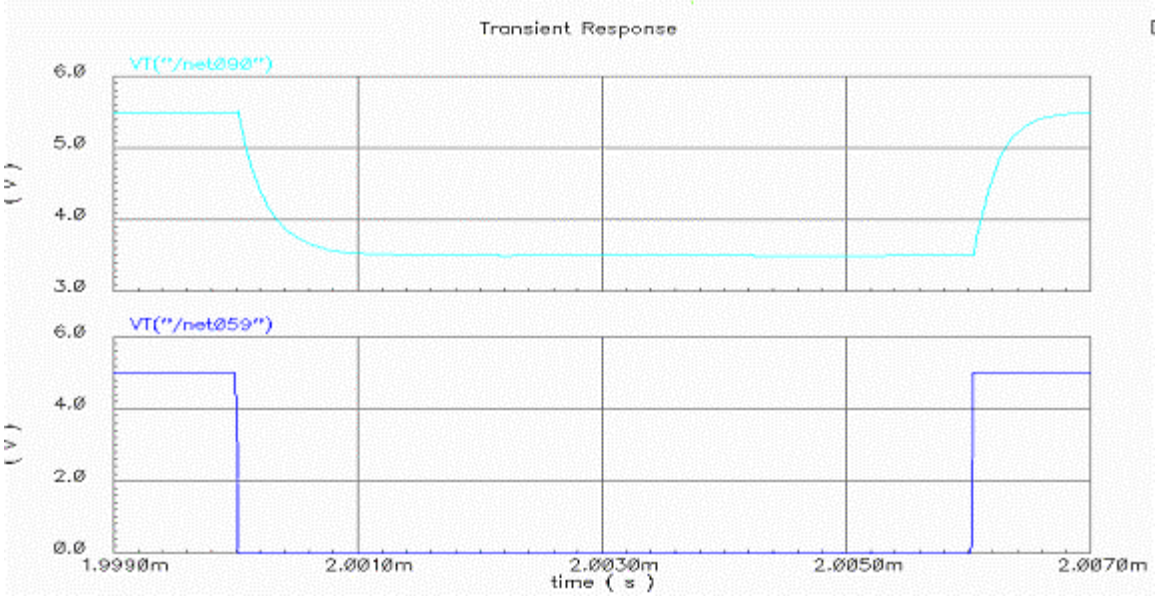


Figure 9 : relation between internal and external Vmemory signal. Top curve: internal signal. Bottom curve: external signal Mem_hl.

In figure 9, the external applied signal Mem_hl is a digital signal between 0 and 5V. The generated internal signal switches between 5.5 and 3.5V. Vmem_h and Vmem_l determine these levels.

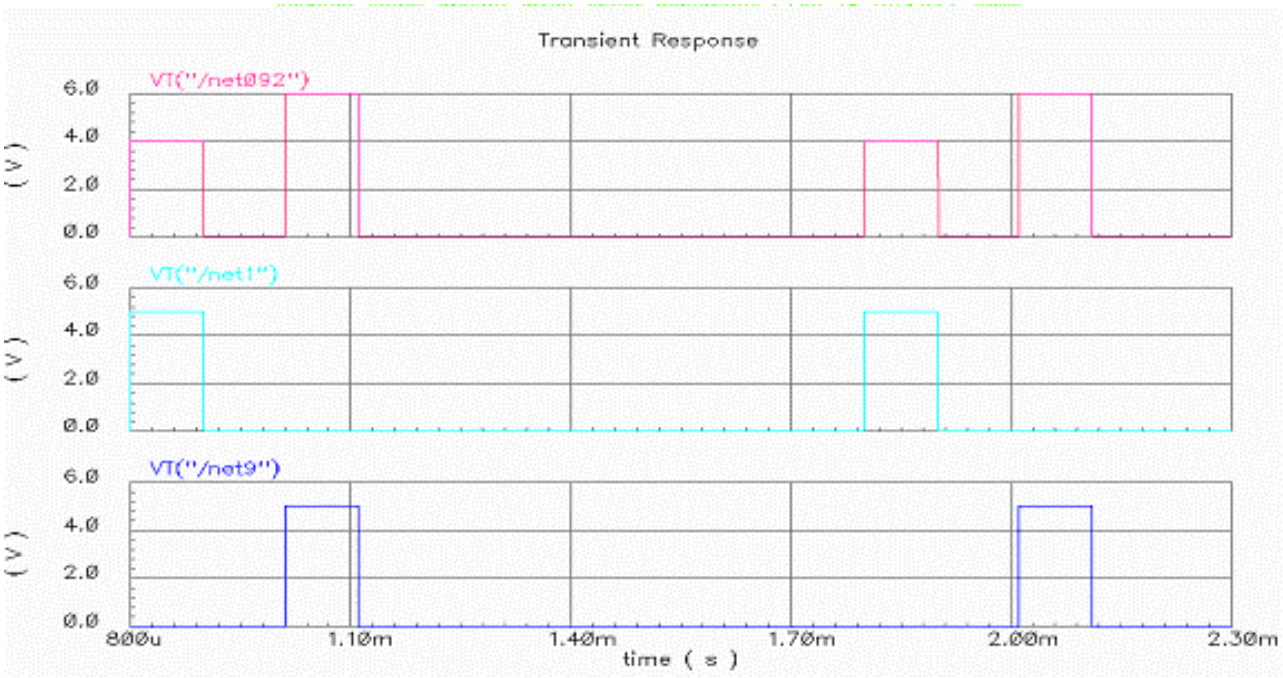


Figure 10 : relation between internal reset signal (top curve) and the external applied reset signals "reset" (bottom curve) and Reset_ds (mid curve)

In figure 10, the reset signal (bottom curve) generates an internal reset pulse of 6V and defines the end and the start of the integration time. This 6V is determined by the supply Vres. If a pulse is given on the Reset_ds signal, a second pulse on the internal reset line is generated to a lower level, determined by the supply Vres_ds. If no Reset_ds pulse is given, the dual slope technique is not implemented.
Note that Reset is dominant over Reset_ds, which means that the high voltage level will be applied for reset, if both pulses occur at the same time.

As one can see from figure 8 and 9, the rise and fall times are not very fast. In fact they are made rather slow to limit the maximum current through the power supply lines (Vmem_h, Vmem_l, Vres, Vres_ds, Vddr). Current limitation of those power supplies is not required.
The external control signals should be capable of driving input capacitance of about 20pF.

4.4 Digital signals

The digital signals control the readout of the image sensor. These signals are :

- Sync_y: Starts the readout of the frame or window at the address defined by the y-address register. This pulse synchronises the y-address register: active high. This signal is at the same time the end of the frame or window and determines the window width.
- Clock_y: Clock of the y-register. On the rising edge of this clock, the next line is selected.
- Sync_x: Starts the readout of the selected line at the address defined by the x-address register. This pulse synchronises the x-address register: active high. This signal is at the same time the end of the line and determines the window length.
- Address: the x- and y-address is downloaded serial through this signal.
- Clock_spi: clock of the serial parallel interface. This clock downloads the address into the SPI register.
- Load_addr: when the SPI register is downloaded with the desired address, the signal Load_addr

signal loads the x-and y-address into their address register as starting point of the window of interest.

- Sh_col: control signal of the column readout. Is only used in sample & hold mode (See timing)
- Norow_sel: Control signal of the column readout. Is only used in Norow_sel mode (See timing)
- Pre_col: Control signal of the column readout to reduce row blanking time
- Sel_active: activates the active load on chip for the output amplifiers. If not used, a passive load can be used or one can use this signal to put the output stages in standby mode.
- Eos_x: end of scan signal: is an output signal, indicating when the end of the line is reached. Is not generated when doing windowing
- Eos_y: end of scan signal: is an output signal, indicating when the end of the frame is reached. Is not generated when doing windowing.

All digital signals are buffered and filtered on chip to remove spikes and to achieve the required on chip driving speed. The applied digital signals should be capable of driving 20pF input capacitance.

4.5 Test signals

Some test signals are required to evaluate the optical performance of the image sensor. Other test signals allow us to test internal modules in the image sensor and some test signals will give us information concerning temperature and influence of the temperature on the black level.

Evaluation on the optical performance (Spectral response, fill factor)

- Array_diode
- Full_diode

Evaluation of the output stages:

- Black
- Dc_black

Evaluation of the x and y –shift registers:

- Eos_x
- Eos_y

Indication of the temperature and influence on the black level:

- Temp_diode_n
- Temp_diode_p

5 Timing

5.1 Timing of the pixel array

The timing of the image sensor can be divided in two major parts. The first part of the timing is related with the timing of the pixel array. This implies the control of the integration time, the synchronous shutter operation, and the sampling of the pixel information onto the memory element inside each pixel. The signals needed for this control are described in previous paragraph 4.3 and figure 7 shows the timing of the internal signals. The relation between the internal and external signals is described in the figure 8, 9 and 10 and should make the timing given in figure 11 clear.

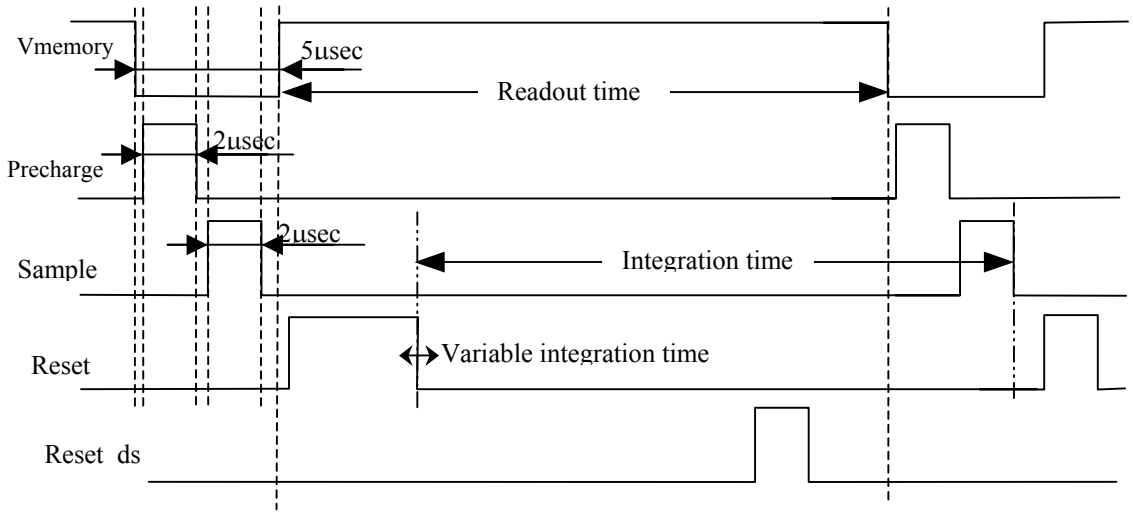


Figure 11: timing of the pixel array. All external signals are digital signals between 0 and 5V. The Reset_ds is only required in case dual slope is desired.

The timing of the pixel array is straightforward. Before the frame is read, the information on the photodiode needs to be stored onto the memory element inside the pixels. This is done by means of the signals Vmemory, Precharge and Sample. Precharge sets the memory element to a reference level and Sample stores the photodiode information onto the memory element. Vmemory pumps up this value to reduce the loss of signal in the pixel and this signal must be the envelop of Precharge and Sample. After Vmemory is high again, the readout of the pixel array can start. The frame blanking time or frame overhead time is thus the time that Vmemory is low, which is about 5µsec. Once the readout starts, the photodiodes can all be initialised by reset for the next integration time. The duration of the reset pulse indicates the integration time for the next frame. The longer this duration, the shorter the integration time becomes. Maximum integration time is thus the time it takes to readout the frame, minus the minimum pulse for reset, which can be about 2µsec. The minimal integration time is the minimal time between the falling edge of reset and the falling edge of sample. Keeping the slow fall times of the corresponding internal generated signals, a minimal integration time is about 2µsec.
An additional reset pulse can be given during integration by Reset_ds to implement the double slope integration mode. (See paragraph 6.1)

5.2 Readout of the pixel array

Once the photodiode information is stored into the memory element in each pixel, the total pixel array of 1280 * 1024 needs to be readout in less than 2 msec (2msec – frame overhead time = 1995µsec). Additionally, it is possible that only a part of the whole frame is read out. This is controlled by the starting address that has to be downloaded and from the end address, which is controlled by the synchronisation pulses in x- and y direction.
The readout itself is straightforward. Line by line is selected by means of a sync-pulse and by means of a Clock_y signal. Once a new line selected, it takes a while (row blanking time) before the information of that line is stable. After this row blanking time the data is multiplexed in blocks of 16 to the output amplifiers. A sync-pulse and a clock pulse in the x-direction do this multiplexing.
Figure 12 shows the y-address timing. The top curves are the selection signals of the pixels, which are sequentially active, starting by the sync pulse. The next line is selected on the rising edge of Clock_y. It is important that the Sync_y pulse covers 1 rising edge of the Clock_y signal. Otherwise the synchronisation will not work properly.

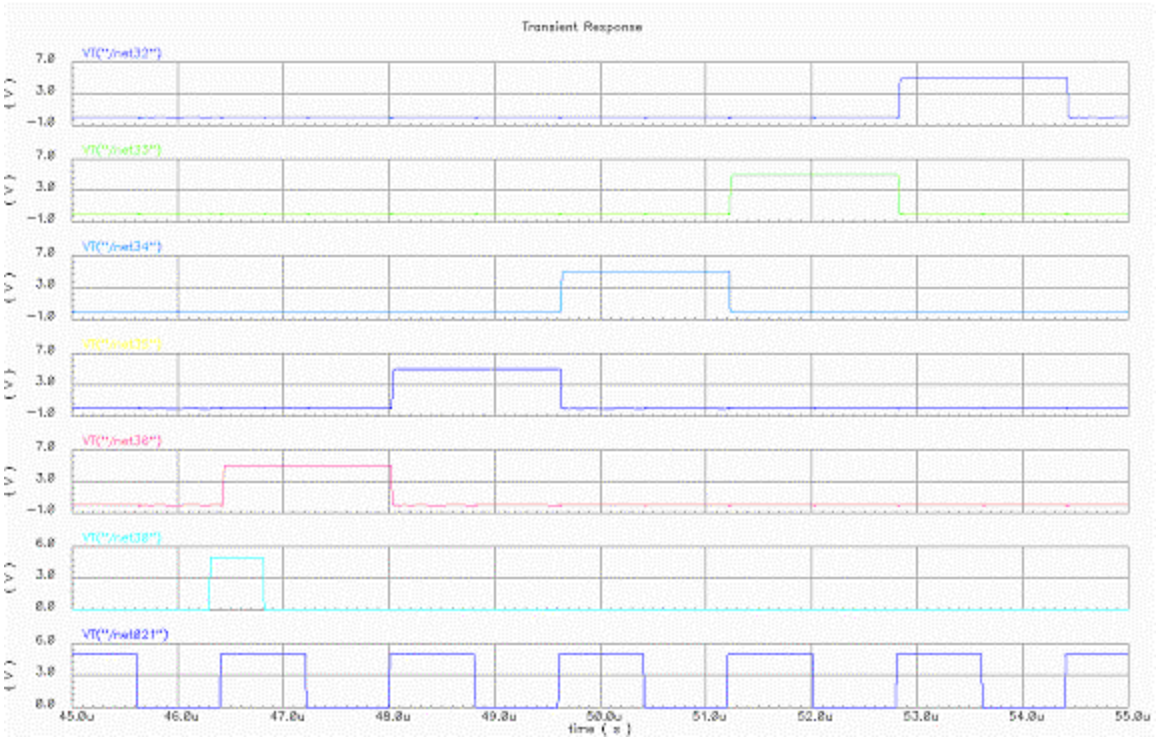
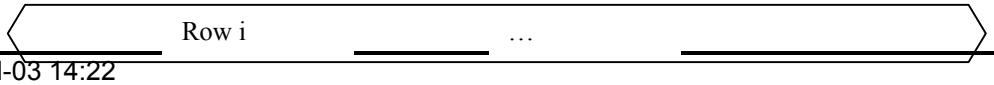


Figure 12 : timing of the y shift register. From bottom to top : Clock_y, Sync_y, Sel_row1, sel_row2, sel_row3, sel_row4, sel_row5.

The sel_row signals are internally generated signals. The first selected line after a Sync_y pulse is the line defined by the y-address in the y-address register. Every select line is in principle 1 clock period long, except for the first select line. The first select line goes high as soon as a Sync_y pulse occurs together with a rising edge of Clock_y. On the next rising edge of Clock_y, the next row is selected, unless Sync_y is still active. In figure 12, a short Sync_y pulse makes sure that the first row is selected during 1 period of Clock_y.

Once a line is selected, it needs to stabilize first of all, which is called the row blanking time, and secondly the pixels needs to be read out. Figure 13 shows the principle.



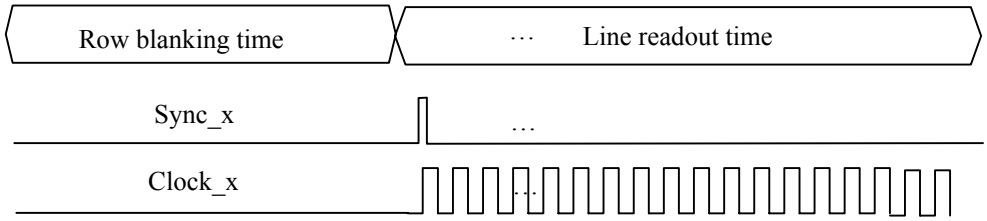


Figure 13 : Readout time of a line is the sum of the row blanking time and on the line readout time.

The row blanking time is a critical time as this has a direct impact on the required pixel rate to obtain 450 frames/sec. On the LUPA design we have integrated 2 different modes to reduce this row blanking time : the baseline SH mode and a new method, named Norow_sel mode. Figure 14 and 15 shows the timing of both modes. In the latter shorter row blanking time, reduced power dissipation and increases dynamic range will be the case, if working properly.

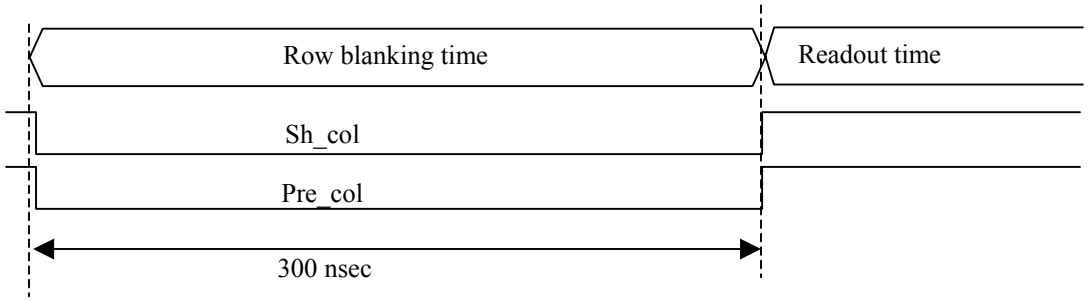


Figure 14 : mode sh_col. The signal Norow_sel is not active (low)

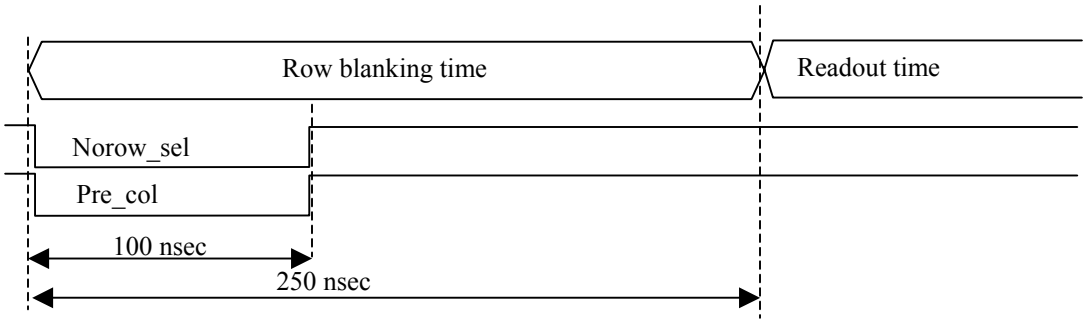


Figure 15 : Mode Norow_sel. The signal Sh_col is continuously active low. A minimum row blanking time of 150 nsec should be possible, by having Norow_sel and Pre_col pulses of 50 nsec.

Once the information of the selected line is stable the addressing of the pixels can start. This is done by means of a Sync_x and a Clock_x pulse in the same way as the Y-addressing. The Sync_x pulse downloads the address in the address register into the shift register and connects the first block of 16 columns to the 16 outputs.
In fact on chip is a 32-output bus instead of 16, but on the rising edge of Clock_x the first 16 columns of the bus are connected to the output stages. On the falling edge of Clock_x, the last 16 columns of the selected bus are connected to the output stages.

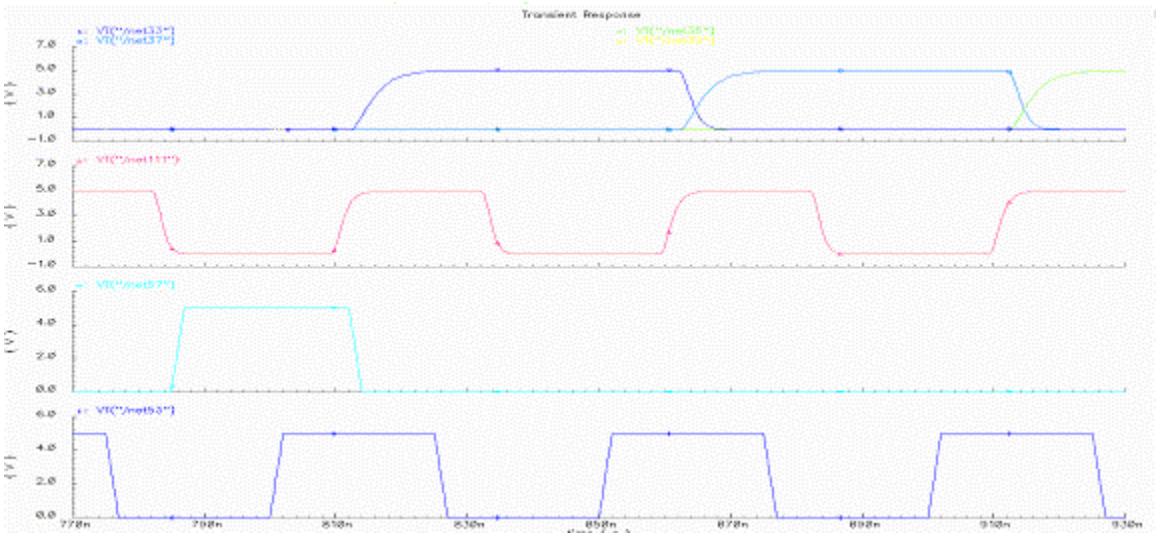


Figure 16: Timing of the x-shift register. The curves from bottom to top : Clock_x, Sync_x, Internal generated Clock, Sel_block1, sel_block2,…

The timing in figure 16 is comparable with the timing of the y-shift register, only that the timing is much faster. Again the synchronisation pulse must be high on the rising edge of Clock_x.

IMPORTANT note : The applied Clock_x, is filtered on chip to remove spikes. This is especially required at these high speeds. This filtering results in an on chip Clock_x that is delayed in time with about 10nsec. In other words, the data at the output has, with respect to the external Clock_x, a propagation delay of 20nsec. This 20nsec come from 10nsec of the generation of the internal Clock_x and 10nsec due to other on chip generated signals.

5.3 Frame rate calculation

The frame period of the LUPA-1300 sensor can be calculated as follows:

Frame period = FOT + (Nr.Lns* (RBT + pixel period * Nr. Pxs / 16)

with: FOT: Frame Overhead Time = 1 us.
Nr. Lns : Number of Lines read out each frame (Y).
Nr. Pxs: Number of pixels read out each line (X).
RBT: Row blanking time = 200 ns (nominal; can be further reduced).
Pixel period: clock_x period/2 (both rising and falling edge are active edges).

Example read out of the full resolution at nominal speed (40 MHz pixel rate):

Frame period = 1 us + (1024 * (200 ns + 25 ns * 1280 / 16) = 2.25 ms => 444 fps.

5.4 Timing of the Serial Parallel Interface (SPI)

The serial parallel interface is used to upload the x- and y-address into the x- and y-address registers. This address is the starting point of the window of interest and is uploaded in the shift register by means of the corresponding synchronization pulse.

The elementary unit cell of the serial to parallel interface is shown in Figure 17. 16 of these cells are

connected in parallel, having a common Load_addr and Clock_spi form the entire uploadable address block. The uploaded addresses are applied to the sensor on the rising edge of signal Load_addr.

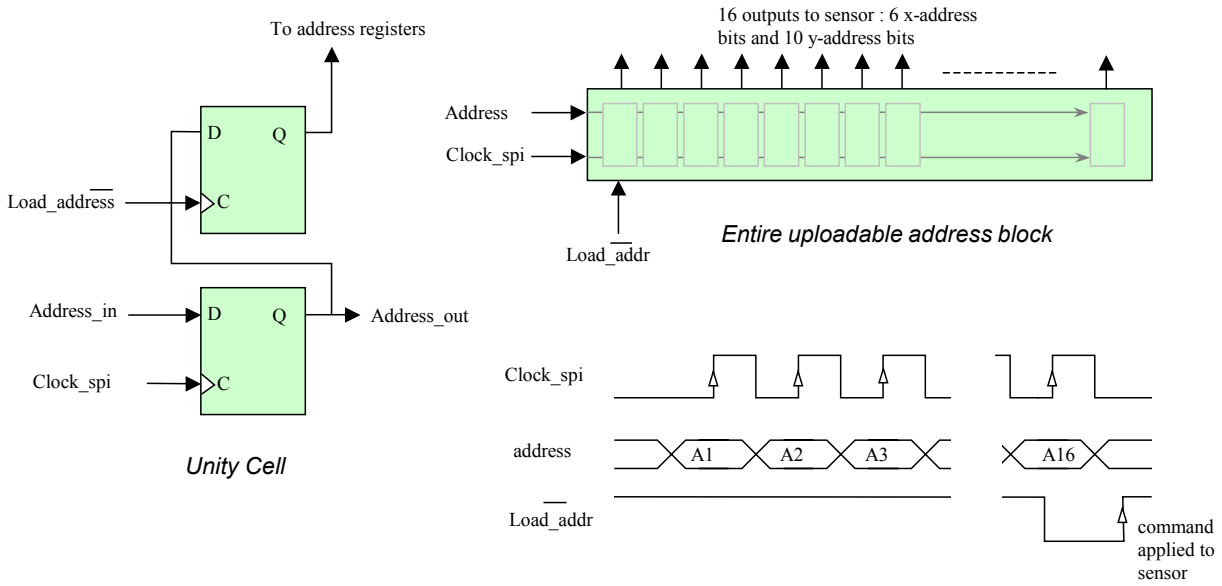
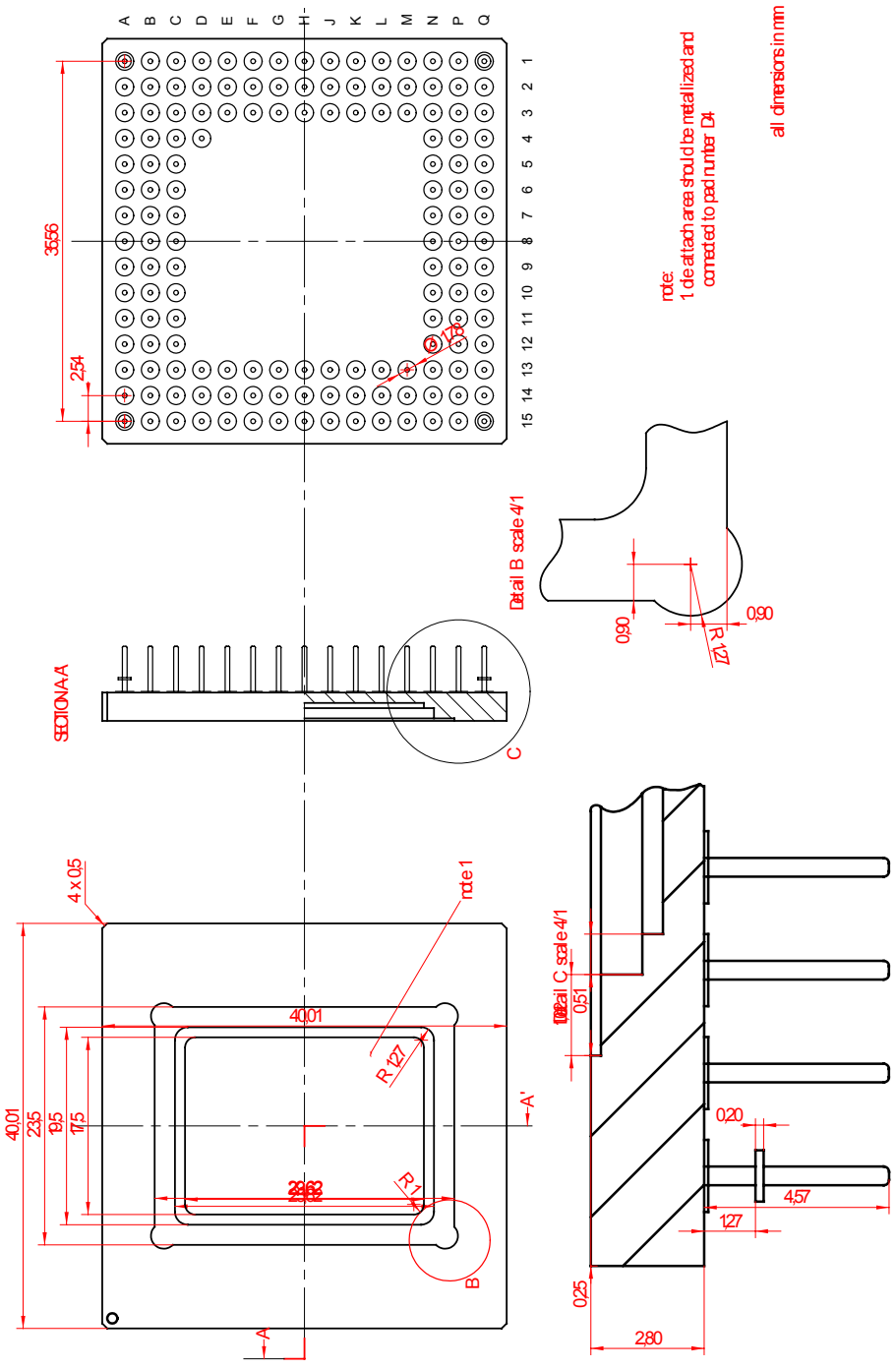


Figure 17 : Schematic of the SPI interface

The Y-address has to be applied first and the X-address last. With respect to the timing in figure 17, A1 corresponds with the least significant bit of the Y-address (Y0) and A16 corresponds with the most significant bit of the X-address (X5). The Y-address is a 10 bit and the X-address is a 6 bit address register.



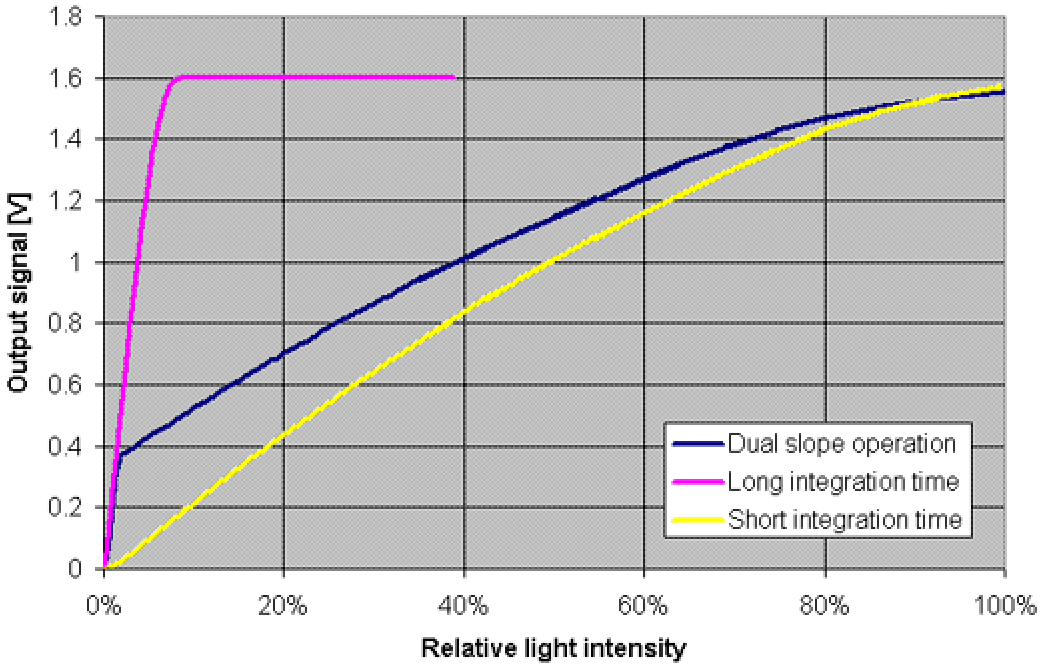
Package information

6 Application notes & FAQ

Q: Can the LUPA1300 directly drive an ADC?
A: Yes, coupling the LUPA to a set of 16 ADC's close to the chip is the preferred way of operation. A suitable ADC must have thus

- Input range equal or larger than the 1.2 V- 0 V sensor signal swing
- In view of the LUPA's S/N 10 bits are suitable. 11 or 12 bits may be considered too.
- Input capacitance 20 pF or lower (high output loads will limit the speed). And no significant resistive loading.
- Sampling frequency 40 MHz (or the application specific sample rate)
- The ADC's input bandwidth must be sufficiently higher than the sampling frequency, in order to avoid RC contamination between successive pixels.

Q: How does the dual slope extended dynamic range mode works?
A: Dual slope is a method to extend the dynamic range of a normally linear-transfer imager, by combining the images taken with a long integration time (dark areas of a scene) and a short integration time (bright areas of a scene) into one image. The resulting electro-optical transfer curve is bi-linear. Multiple slope is an extension of it, resulting in a multi-linear transfer curve with multiple knee points.



Please look at our website to find some pictures taken with the double slope mode on:
http://www.fillfactory.be/htm/technology/htm/dual-slope.htm

APPENDIX A: LUPA-1300 Evaluation kit

For evaluating purposes a LUPA-1300 evaluation kit is available.

The LUPA-1300 evaluation kit consists of a multifunctional digital board (memory, sequencer and IEEE 1394 Fire Wire interface), an ADC-board and an analog image sensor board.

Visual Basic software (under Win 2000 or XP) allows the grabbing and display of images and movies from the sensor. All acquired images and movies can be stored in different file formats (8 or 16-bit). All setting can be adjusted on the fly to evaluate the sensors specs. Default register values can be loaded to start the software in a desired state.

Please contact Fillfactory (info@Fillfactory.com) if you want any more information on the evaluation kit.

(EOD)